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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PAUL PETERSEN

Appeal 2008-0770
Application 09/419,523
Technology Center 2100

Decided:[1] April 27, 2009

Before JAMES D. THOMAS, JOSEPH L. DIXON,
and JEAN R. HOMERE, *Administrative Patent Judges*.

THOMAS, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 CFR § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Data (electronic delivery).

STATEMENT OF THE CASE

This is appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 41 through 51, 53 through 60, 62 through 65, and 67. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Invention

Appellant's invention relates to determining memory upgrade options in a computer system. The focus is upon executing software to determine a maximum number of memory devices that can be supported by each memory bus channel of the computer system and to determine the maximum number of device sockets that can be supported by a memory controller of the system. (Figures 1 and 3, Summary, Spec. 1-2.)

Representative Claim

41. A method to provide memory upgrade information comprising:

obtaining memory configuration information of a computer system;

determining a memory capacity of the computer system, including executing a software routine to determine a maximum number of memory devices that can be supported per memory bus channel of the computer system; and

automatically determining memory upgrade options based on the determined memory capacity of the computer system.

Prior Art and Examiner's Rejections

The Examiner relies upon the following references as evidence of unpatentability:

Helm	US 5,129,069	Jul. 7, 1992
Arai	US 5,280,599	Jan. 18, 1994
Dresser	US 5,446,860	Aug. 29, 1995
Yoshizawa	US 5,787,464	Jul. 28, 1998
Cowell	US 5,860,134	Jan. 12, 1999

Ware, Frederick, "Direct RMC.d1 Data Sheet", RAMBUS, DL0036-00.7 (Aug. 7-13, 1998), pp. 1-104.

All claims on appeal, claims 41 through 51, 53 through 60, 62 through 65, and 67 stand rejected under 35 U.S.C. § 103. In a first stated rejection of claims 41, 42, 45, 48, 49, 51, 53 through 55, 58 through 60, 62 through 65, and 67, the Examiner relies upon Arai in view of Yoshizawa, further in view of Ware that is cited as extrinsic evidence of inherency according to the reasoning in the final rejection and at page 7 of the Answer. To this initial combination of references, the Examiner adds Helm as to claims 43, 56, and 57 in a second stated rejection. Furthermore, the Examiner utilizes the initial combination of references, further in view of Cowell as to claims 44 in a third stated rejection. Lastly, in a fourth stated rejection, the Examiner relies upon the initial combination of references, further in view of Dresser as to claims 46, 47, and 50.[2]

[2] The outstanding rejections of all claims on appeal under the enablement and written description portions of the first paragraph of 35 U.S.C. § 112 as set forth in the final rejection have been withdrawn by the Examiner at page 5 of the Answer.

Claim Groupings

Based upon Appellant's arguments in the principal Brief on appeal, we will decide the appeal on the basis of independent claims 41, 54, and 62 which are argued collectively. No arguments are presented as to any dependent claims within the first stated rejection, and no arguments are presented to us in the principal Brief and Reply Brief relative to the second through fourth stated rejections of the remaining dependent claims.

Issue

Has Appellant shown that the Examiner erred in finding that the combination of Arai in view of Yoshizawa, further in view of Ware (RAMBUS) as extrinsic evidence of inherency, teaches the features common to independent claims 41 and 62 of executing a software routine to determine a maximum number of memory devices that can be supported per memory bus channel of a computer system and a corresponding feature in independent claim 54 of computer instructions determining a maximum number of device sockets that can be support by a memory controller?

Prior Decision

Page 4 of the principal Brief and page 4 of the Answer indicates this application was subject to a previous decision on appeal, Appeal No. 2004-0037, mailed on August 31, 2004, in which a previous panel of this Board affirmed the Examiner's rejections of all then appealed claims rejected under

35 U.S.C. § 103. The patents relied on by the Examiner in this prior appeal have also been relied on by the Examiner in this appeal, in addition to the newly added publication to Ware (RAMBUS).

Findings of Fact

1. We incorporate by reference the discussion at pages 4 through 8 of our prior decision where we discussed in detail corresponding, respective teachings of Arai and Yoshizawa and concluded that they were properly combinable within 35 U.S.C. § 103. With specific reference to Arai, the discussion detailed various figures and written description portions of Arai's patent that discussed the software basis of determining memory capacity according to his teachings. To a lesser extent, we made similar observations with respect to Yoshizawa. Additionally, the latter reference has plural embodiments of an overall system in figure 1. In accordance with the discussion in the paragraph bridging columns 2 and 3 of Yoshizawa, the showing in figure 2 illustrates "[m]emories 201 and 202 contain operating systems (hereinafter referred to as "OS") 206 and 211, have memory extraction/insertion support means 207 and 212, memory copying means 208 and 213 and status management table secured means 209 and 214 as part of the OS program" as stated at column 3, lines 1 through 6. Figure 3 shows the flow of the processing at the memory extraction/insertion support means. According to various other embodiments, various other flow charts of software processing flows are illustrated in subsequent figures.

2. The Examiner states the following at pages 10 and 11 of the Answer:

> As for 'executing a software routine to determine a maximum number of memory devices that can be supported per memory bus channel of the computer system,' this was a well known technique used to determine total memory capacity in prior art computer systems and was 'readily understood by one of ordinary skill in the art', as conceded by appellant on page 10 of the Appeal Brief. RAMBUS is cited as extrinsic evidence of such, as disclosed on the top of page 40 of RAMBUS, wherein address values were programmed into configuration fields to determine total device size. Page 41 discloses configuration. Page 42 discloses initialization (software routine) that determines present devices. Page 40 discloses that a device field has been programmed at 5-bits, therefore allowing maximum of 32 devices per stick. Pages 56-58 further disclose configuration and RDRAM initialization. Also, see page 73, which discloses the algorithm InitDev. The system must determine whether it is actually there or not (a characteristic other than size). Whether it is present or not will affect the capacity. This is discussed in RAMBUS on page 1, which discloses the optional 1 to 32 RDRAMS that may be connected to the controller, page 40, which discusses the configuration options (number of regions, e. g.), page 41, which discusses the addressing options based on the configuration, page 42, which discloses that initialization "automatically" (i.e., using a configuration routine including instructions to obtain memory configuration information) manages the configuration, including whether a device is present or not, page 45, which elaborates on the mapping techniques, page 57, which shows the actual configuration commands for the number of devices present, and pages 72-75, which discuss initialization of the devices, including "serial presence detect."

Analysis

At the outset, we note that page 5 of the principal Brief indicates that claims 41 through 51, 53 through 60, 62 through 65, and 67, all claims on appeal, are the subject of the present appeal. As indicated first at page 9 of

the principal Brief and in detail beginning at page 11 of this Brief, Appellant presents arguments only as to the subject matter presented in independent claims 41, 54, and 62 within the first stated rejection under 35 U.S.C. § 103. Since we affirm the rejection of these claims, we also affirm the rejection of the remaining dependent claims within this first stated rejection as well as the second through fourth stated rejections which, as indicated earlier in this opinion, have not be argued separately as well.

Appellant's arguments presented at pages 12 and 13 of the principal Brief on appeal do not argue that Arai and Yoshizawa are not properly combinable within 35 U.S.C. § 103 and Appellant does not contest the Examiner's reliance upon Ware (RAMBUS) as being extrinsic evidence of inherency. Rather, the arguments here only take the general view that the combination of teachings does not teach all the limitations of independent claims 41, 54, and 62 on appeal, and only present specific arguments set forth in the issues section in this opinion with respect to them. We note here as well that we previously found at pages 4 through 8 of the prior decision with respect to this application that Arai and Yoshizawa were properly combinable within 35 U.S.C. § 103 anyway.

We do not agree with Appellant's urgings at pages 12 and 13 of the principal Brief that the combination of teachings of Arai and Yoshizawa does not teach the ability to determine the maximum of number of memory devices at any point in time that "can" be supported by a memory channel and by a respective controller to include device sockets to which they are attached. It appears to us that our prior decision as expanded upon in finding of fact 1 makes this very clear to begin with. Furthermore, the Examiner's

responsive arguments in finding of fact 2 are extensive and amplify the corresponding teachings in Ware (RAMBUS) which are not contested in the Reply Brief.

As to this Reply Brief, we will not consider the arguments presented from page 1 through the middle of page 7, since they are considered untimely and have essentially been waived since the combinability argument has not been raised initially in the principal Brief on appeal. The filing of a Reply Brief is not to be construed as permission to present arguments that should have been raised in the principal Brief on appeal.

On the other hand, the arguments presented at pages 7 and 8 of the Reply Brief are misplaced since the combinability of the teachings of Arai and Yoshizawa has already been determined to be proper within 35 U.S.C. § 103 from our prior decision, including for the present claims on appeal.

Appellant's arguments at pages 8 and 9 of the Reply Brief are directed to the Examiner's initial arguments presented at the bottom of page 10 of the Answer, the initial portion of which we reproduced in finding of fact 2. The Examiner properly referred to admissions made by Appellant at the bottom of page 10 of the principal Brief on appeal. In this respect, according to the disclosed invention, the determination of the maximum number of memory devices or sockets that may be added to a memory bus or controller was admitted to be known in the art, but it was taught to be storable in a non-volatile storage device according to the disclosed invention. What is very telling in these remarks in this portion of the Reply Brief is the failure to consider all the arguments that we reproduced from the Examiner in finding of fact 2. The examiner explained in detail pertinent, significant teachings in

Ware (RAMBUS) which make clear to the reader that through the combined teachings of Arai and Yoshizawa within 35 U.S.C § 103, with the teachings of RAMBUS as extrinsic evidence of inherency, software routines were known in the art to determine the maximum number of devices that can be supported by a memory channel according to independent claims 41 and 62 on appeal, as well as the corresponding feature of instructions to determine the maximum number of device sockets that can be supported by a memory controller according to independent claim 54.

Thus, on the basis of the weight of the arguments and evidence before us, the Examiner's conclusion of the obviousness of the subject matter of independent claims 41, 54, and 62 on appeal is well supported.

Conclusion of Law

Appellant has not shown that the Examiner erred in finding that the combination of Arai and Yoshizawa, with the additional extrinsic evidence from Ware (RAMBUS), teaches the disputed features common between independent claims 41 and 62 on appeal and the corresponding feature of independent claim 54 on appeal.

DECISION

The Examiner's four separately stated rejections, encompassing all claims on appeal, based upon 35 U.S.C. § 103 are affirmed. All claims are unpatentable.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. §1.136(a). See 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

pgc

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